ARYA COLLEGE OF ENGINEERING
GUESS PAPERS
(B. Tech. II Year III Semester 2025-26)

3CS3-04/ 3CCS3-04/3IT3-04: Digital Electronics: Dr. Abha Sharma

Unit 1:

Short Answers: (2 Marks Each)

Q. 1 Convert the numbers into desired base.
(i) (A6BF5)16 = ( )2
(ii) (101.01)2 = ( )10
(iii) (7.FD6) 16 = ( )8
(iv) (7864) 10 = ( )16
(v) (643)10 into Excess-3 code.
(vi) (10110)2 into gray code.
(vii) Gray code 110101 to binary form.
Q. 2 Subtract 748 from 983 using 9's complement method.
Q. 3 Add following using the 2's complement method (i) -48 and +31 (ii) -32 and -16 (iii) +38 and -22
Q. 4 Convert the gray code 110101 to binary form.
Q. 5 Convert $(643)_{10}$ into Excess-3 code and (10110)2 into Gray code.
Q. 6 What are logic gates. Explain Universal logic gates.
Q. 7 What is truth table. Write the truth table and symbolic representation of each logic gate.
Q. 8 What do you understand with 1's and 2's complement method of subtraction. Which method is efficient and why?

Descriptive Answers: (5 to 20 Marks)

Q.1 Write a short note on weighted and non-weighted codes, Binary codes, Gray codes, Excess-3 codes.
Q.2 Explain the reflected code.
Q.3 Realize all logic gates through universal gates.
Q.4 What is digital System. Write the characteristics of Digital System.

Unit 2:

Short Answers: (2 Marks Each)

Q.1 State De Morgan's theorem.
Q.2 What is the basic law of Boolean algebra?
Q.3 Define Minterm and Maxterm, SOP AND POS.
Q.4 Verify the following operations are commutative but not associative. (i) NAND (ii) NOR
Q.5 Define Prime Implicants, Essential Prime Implicant and reduced Prime Implicants.
Q.6 Name the universal gate with their truth table and logic symbol. Why these gates are called Universal gates.

Descriptive Answers: (5 to 20 Marks)

Q.1 Simplify (a) y'z'+w'x'z'+w'xyz'+wyz'
(b) A'B+AC+BC'+B'C+AB
Q. 2 Simplify F(A,B,C,D) =∑(0,2,3,5,7,8,9,10,11)+d(4,15) using Tabular method.
Q. 3 Simplify Y=∑(3,6,7,8,10,12,14,17,19,20,21,24,25,27,28) using K-map method.
Q. 4 Express the Function Y=A+B'C in (a) Canonical SOP form (b) Canonical POS form
Q. 5 Obtain (a) minimal sop and (b) minimal pos for the function
Y=∑(0,1,2,5,8,9,10)
Q. 6 If A'B+CD'=0, Then prove that
AB+C'(A'+D') =AB+BD+B'D'+A'C'D
Q. 7 write the difference between Tabular method and K-Map.

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Unit 3:

Short Answers: (2 Marks Each)

Q.1 What is meant by logic family?
Q.2 What is a tri state gate?
Q.3 Draw the diagram of Diode Transistor logic?
Q.4 What is MOSFET? Name the different types of MOSFET.
Q.5 Why ECL logic is faster than TTL?
Q.6 What is Noise margin.

Descriptive Answers: (5 to 20 Marks)

Q.1 Explain the working of TTL Tri state output.
Q.2 Write notes on (i) Noise Immunity (ii) Fan in (iii) Speed of operation (iv) Propagation Delay
Q.3 Draw and explain the working of Emitter coupled logic?
Q.4 Draw and explain the working of CMOS NAND & NOR gate?
Q.5 Explain with the aid of a circuit diagram of Register transistor logic.
Q.6 What do you mean by Digital system? Explain its characteristics.
Q.7 Compare all logic families with its characteristics.

Unit 4:

Short Answers: (2 Marks Each)

Q.1 What is half adder? Write its truth table.
Q.2 What is full adder? Draw its circuit with Half adders and NAND gates only.
Q.3 What is multiplexer? Draw the circuit of 64x1 Mux.
Q.4 What is de multiplexer?
Q.5 What is meant by a decoder? Draw the block Diagram of decoder.
Q.6 Design full subtractor using basic gate.

Descriptive Answers: (5 to 20 Marks)

Q.1 Explain the BCD to Seven segment decoder.
Q.2 What is BCD adder. Explain the steps to add two BCD number.
Q.3 Implement a 16 to 1 multiplexer using 4 to 1 multiplexer.
Q.4 Explain the working of Half and Full Adder and Subtractor using NAND gates with their truth table and circuit diagram.
Q.5 Explain the working of Binary to gray converter and Gray to Binary code converter.
Q.6 What is Encoder & Decoder Circuits? Explain the working of octal to binary encoder.
Q.7 Implement the following function using 4x 1 multiplexer. f (A, B, C) = Σ0,1,4,7) use A and B as select lines.
Q.8 Implement full subtractor using 3 to 8 decoders.

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Unit 5:

Short Answers: (2 Marks Each)

Q.1 What is Flip Flop?
Q.2 Define the difference between Latch and Flip flop.
Q.3 What is Counter? Explain with its types.
Q.4 What is Shift Register? Name the different types of Shift Registers.
Q.5 List four basic Flip-Flop with truth table and excitation table and applications.
Q.6 Differentiate between Combinational circuit and Sequential circuits with examples.
Q.7 What is the difference between Synchronous and Asynchronous Counter?
Q.8 What is the propagation delay in Ripple counter. Calculate frequency of 3-bit counter having flip flops identical propagation delay of 100 ns.

Descriptive Answers: (5 to 20 Marks)

Q.1 Realize SR Flip Flop using J-K and D flip Flop.
Q.2 What is Race around Condition? How can we Eliminated this. Explain the working of Master Slave flip flop with diagram.
Q.3 Describe the Parallel In serial out shift register with neat logic diagram.
Q.4 Draw and explain the working of 4-bit Asynchronous Counter (Ripple).
Q.5 Design a Mod-10 counter using J-K Flip Flop.
Q.6 Describe the serial in serial out shift register with neat diagram.
Q.7 Explain in short Universal shift Register and Bi-directional Shift Register.
Q.8 Design asynchronous Up Down Counter using FF.
Q.9 Draw & explain the following with a truth table & logic circuit diagram:
(a) S-R Flip Flop (b) D Flip Flop (c) J-K Flip Flop (d) T Flip Flop